CLAIMS

1. A buffer manager, comprising:

an input for receiving packets of data, each packet associated with an output queue;

an intermediate storage facility having a plurality of blocks;

an intermediate storage facility manager configured to assign particular blocks of the intermediate storage facility to output queues, and store one or more packets associated with the output queues into the blocks assigned to those output queues.

2. A buffer manager according to claim 1 wherein the intermediate storage facility manager comprises:

a pointer repository for tracking locations in the intermediate storage facility;

a trunk manager configured to interact with the pointer repository to store locations of trunks stored in the intermediate storage facility.

3. A buffer manager according to claim 2 wherein each trunk managed by the trunk manager is made of one or more blocks of the intermediate storage facility having a common output queue.

4. A buffer manager according to claim 2 wherein the intermediate storage facility manager further comprises a temporary storage memory circuit for storing the packets of data prior to the time that the packets of data are stored in the intermediate storage facility.

5. A buffer manager according to claim 1 wherein the intermediate storage facility is an SRAM circuit.

6. A buffer manager according to claim 1 wherein the output queue is a virtual output queue.

7. A buffer manager according to claim 1, further comprising:

a second storage facility able to store groups of blocks that were previously stored in the intermediate storage facility;

a second storage facility manager coupled to the intermediate storage facility manager and configured to accept a command from the intermediate storage facility manager and, upon

receipt of the command, store into the second storage facility one or more groups of blocks that were previously stored in the intermediate storage facility.

8. A buffer manager according to claim 7 wherein the second storage facility manager comprises:

a memory access controller coupled to the second storage facility;

a memory bank scheduler coupled to the memory access controller and configured to direct portions of groups of blocks to particular banks of the second storage facility.

9. A buffer manager according to claim 8, wherein the second storage facility manager comprises a dynamic balancer, including:

a token register including a number of tokens,

a token distributor configured to allocate the number of tokens between read and write process managers,

the write process manager configured to accept a number of write tokens from the token distributor and authorize a number of data write operations to the second storage facility equal to the number of write tokens received, and

the read process manager configured to accept a number of read tokens from the token distributor and authorize a number of data read operations to the second storage facility equal to the number of read tokens received.

10. A buffer manager according to claim 9 wherein the dynamic balancer is configured to force all of the number of data write operations to be performed before any of the data read operations are performed.

11. A buffer manager according to claim 7, further comprising an output queue manager configured to supervise output queues made of one or more trunks.

12. A buffer manager according to claim 7 wherein the second storage facility is an SDRAM circuit.

13. A buffer manager according to claim 7, further comprising a third storage facility coupled to the second storage facility manager, the third storage facility able to store groups of blocks that were previously stored in the second storage facility.

14. A buffer manager according to claim 7, further comprising:

an output SDRAM storage circuit;

an output SDRAM controller coupled to the second storage facility manager, the output SDRAM controller circuit configured to store trunks of data that were previously stored in the second storage facility.

15. A line interface card, comprising:

one or more input ports configured to receive packets;

one or more output ports configured to transmit packets; and

a packet buffer manager, including

a buffer memory having blocks of storage locations;

a buffer memory manager configured to sort the data packets into groups and store the groups into the buffer memory blocks.

16. A line interface card according to claim 15 wherein the data packets are sorted into groups having common assigned output queues prior to being stored into the buffer memory blocks.

17. A line interface card according to claim 15, further comprising:

a block storage memory; and

a block storage memory manager coupled to the buffer memory manager.

18. A line interface card according to claim 17 wherein the block storage memory manager comprises:

a memory access controller coupled to the block storage memory;

a memory bank scheduler coupled to the memory access controller and structured to direct portions of the one or more groups of blocks to particular banks of the block storage memory.

19. A line interface card according to claim 17, further comprising a second block storage memory coupled to the buffer memory manager, the second block storage memory able to store groups of blocks that were previously stored in the block storage memory.

20. A line interface card according to claim 17, further comprising:

an output SDRAM storage circuit;

an output SDRAM controller coupled to the block storage memory manager, the output SDRAM controller circuit structured to store trunks of data that were previously stored in the block storage memory.

21. A line interface card according to claim 15 wherein the computer network is the Internet.

22. A line interface card according to claim 15 wherein the buffer memory manager further comprises a temporary storage memory circuit for storing the packets of data prior to the time that the packets of data are stored in the buffer memory.

23. A line interface card according to claim 15, further comprising a packet processor coupled to one or more of the input ports and output ports.

24. A network device, comprising:

one or more input ports;

one or more output ports;

a switching fabric connecting selected input ports to selected output ports;

a packet buffer manager, including

a buffer memory having a plurality of storage location blocks,

a buffer memory manager configured to sort data packets accepted from the input ports into groups and store the groups into one or more of the plurality of the storage location blocks in the buffer memory; and

a scheduler configured to direct the packet buffer manager to output the groups through the switching fabric.

25. A network device according to claim 24 wherein the buffer memory manager is configured to sort the data packets accepted from the one or more input ports into groups having a common output queue.

26. A network device according to claim 25, further comprising a block storage memory, and wherein the buffer memory manager is coupled to a block storage memory manager.

27. A network device according to claim 26 wherein the block storage memory manager is configured to accept a command from the buffer memory manager and, upon receipt of the command, store into the block storage memory one or more groups of blocks that were previously stored in the buffer memory.

28. A network device according to claim 26 wherein the block storage memory manager comprises:

a memory access controller coupled to the block storage memory;

a memory bank scheduler coupled to the memory access controller and configured to direct portions of groups of blocks to particular banks of the block storage memory.

29. A network device according to claim 26, further comprising a second block storage memory coupled to the buffer memory manager, the second block storage memory able to store groups of blocks that were previously stored in the block storage memory.

30. A network device according to claim 26, further comprising:

an output SDRAM storage circuit;

an output SDRAM controller coupled to the block storage memory manager, the output SDRAM controller circuit structured to store trunks of data that were previously stored in the block storage memory.

31. A network device according to claim 24 wherein the computer network is the Internet.

32. A network device, comprising:

one or more input ports structured to accept data packets from a computer network, each packet having an assigned output queue;

one or more output ports structured to send data packets onto the computer network;

a switching fabric coupled to the one or more input ports and the one or more output ports and structured to connect selected input ports to selected output ports;

a packet buffer manager, including

an input coupled to the one or more input ports,

a buffer memory having a plurality of storage location blocks, each block able to store at least a portion of the data packets accepted from the one or more input ports,

a buffer memory manager structured to sort the data packets accepted from the one or more input ports into groups, store the groups into one or more of the plurality of the storage location blocks in the buffer memory, and retrieve one or more of the stored groups; and

a scheduler coupled to the packet buffer manager and to the switching fabric, the scheduler structured to direct the packet buffer manager to read one or more of the stored groups and to direct the groups read from the buffer memory through the switching fabric.

33. A network device according to claim 32 wherein the buffer memory manager is structured to sort the data packets accepted from the one or more input ports into groups having a common output queue.

34. A network device according to claim 33, further comprising a block storage memory, and wherein the buffer memory manager is coupled to a block storage memory manager.

35. A method for buffering packet data in a network device, comprising:

receiving data packets at an input port, each data packet having a predetermined output queue;

aligning the data packets into groups of packets each having the same output queue; and

storing the grouped data packets together in blocks of a memory device.

36. A method for buffering packet data according to claim 35, further including creating a list of the blocks used to store the grouped data packets having the same output queues.

37. A method for buffering packet data according to claim 35, further comprising, upon receiving a signal:

reading predetermined grouped data packets previously stored in the blocks of the memory device; and

removing the read grouped data packets from the memory device.

38. A method for buffering packet data according to claim 37 that further comprises storing the predetermined grouped data packets in a second memory device after the predetermined grouped data packets have been read from the memory device.

39. A method for buffering packet data according to claim 35 wherein aligning the data packets into groups of packets each having the same output queue comprises:

determining a required number of blocks in the memory device to store the packets having the same output queue;

obtaining addresses of the required number of free blocks in the memory device; and

creating an ordered list of the addresses obtained.

40. A method for buffering packet data according to claim 35 wherein aligning the data packets into groups of packets each having the same output queue comprises:

determining a required number of blocks in the memory device to store the packets having the same output queue;

requesting pointers to the required number of free blocks in the memory device from a free block pool; and

creating a linked list of the pointers obtained from the free block pool.

41. A method for buffering packet data according to claim 35, further comprising:

receiving additional packets at the input port, some of the additional packets having the same output queue as the group of packets previously stored in the memory device;

storing in the memory device the received additional packets having the same output queue as the group of packets previously stored in the memory device; and

relating the memory location of the group of packets previously stored in the memory device to the memory location of the additional packets stored in the memory device.

42. A method for buffering packet data according to claim 41 wherein relating the memory location of the group of packets previously stored in the memory device to the memory location of the additional packets stored in the memory device comprises adding additional pointers to a linked list.

43. A method for buffering packet data according to claim 38 wherein storing the predetermined grouped data packets in a second memory device comprises storing the grouped data packets in an SDRAM memory device as a single unit.

44. A method for buffering packet data according to claim 37 wherein the signal is generated when one of the following conditions is true:

when a pre-set time after storing the grouped data packets together in blocks of the memory device has elapsed; or

when an amount of data stored in the blocks of the memory device equals or exceeds a threshold.